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(54) A differential operational amplifier

(57) A low voltage, broadband differential operational amplifier which eliminates the long tail current source from the amplifier, thereby relieving the headroom requirements by a few tenths of a volt. An input common mode feedback circuit (11) is used to overcome the problems arising from the removal of the long tail current source of prior art circuits. This circuit monitors the common mode feedback current (CMFB) and when the value of the current exceeds a specified range around the nominal amplifier bias current, an appropriate correction in the common mode input voltage (V_{in}) is made. This novel amplifier will be valuable for use in pipelined analog-to-digital converter applications, as well as many other low voltage and/or portable applications.

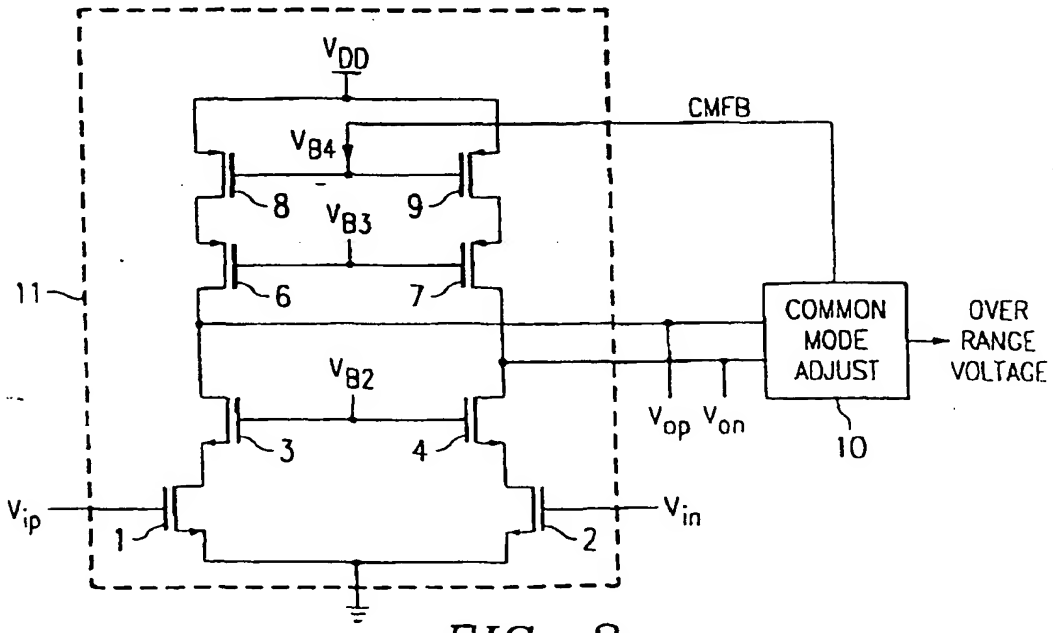

FIG. 2

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Description

[0001] This invention relates to the field of electronic circuits associated with operational amplifiers (op-amps) and in particular to low-voltage versions of these circuits suitable for use in various pipelined analog-to-digital converter and/or other portable applications.

[0002] Figure 1 shows a schematic for the well known 'telescopic cascode' amplifier. A bandwidth of 500 MHz and a dc gain of 60 dB is achievable with this type circuit.

This differential op-amp is comprised of cascoded n-channel input transistors 1,3 and 2,4 at the V_{ip} and V_{in} inputs, respectively, along with the long tail current source transistor 5. P-channel transistors 6-9 act as an active load. The common mode adjust circuitry 10 is used to compensate for a mismatch between tail current and the bias current by providing a common mode feedback (CMFB) signal to the gates of transistors 8 and 9. The differential outputs V_{Op} and V_{On} for the circuit are taken from the drains of n-channel transistors 3 and 4, respectively. Because this amplifier is known to have a minimum number of non-dominant poles, the circuit has excellent bandwidth properties. This is primarily due to the following:

1) the p-channel transistors 6-9 in the circuit do not carry any signal current. Thus, all capacitances associated with p-channel transistors 8 and 9, as well as the gate-source and source-substrate capacitances of p-channel transistors 6 and 7 do not contribute any poles;
2) since the main non-dominant poles are contributed by the n-channel transistors, which can be kept small in size by tailoring their W/L layout for a given transconductance, the resulting poles will generally be at higher frequencies;
3) the large capacitance often associated with a folded cascode amplifier, where three transistors have to 'meet' at the folding node, is not present in this telescopic cascode amplifier.

[0003] The main problem with this conventional cascode operational amplifier circuit is that of low voltage headroom. Because so many transistors are stacked, it is difficult to realize this circuit when working at voltages as low as 2.5 volts or less.

[0004] A number of patents may be of interest in relation to the technology discussed above and in this patent, including but not limited to the following:

U.S. Patent No. 5,798,673 Low voltage operational amplifier bias current and method.
U.S. Patent No. 5,734,296 Low voltage operational amplifier input stage and method.

[0005] The invention provides a differential operational amplifier for operation between a first and a second voltage supply, comprising:

a differential pair of cascoded input transistors including first input means for receiving first and second input signals, active transistor loads for connecting output means of each of said input transistor cascodes to the second voltage supply, and
a common mode adjust circuit connected to adjust the currents in the active transistor loads in accordance with the common mode output signal from the output means of the differential pair of cascoded input transistors, wherein

in the operation of the amplifier, second input means of said cascoded input transistors are coupled directly to the first voltage supply.

[0006] The long-tail current source is eliminated from a differential amplifier in accordance with the invention.

[0007] Preferably, the amplifier includes field effect transistors in the differential pair of cascoded input transistors, the source terminals of the lower field effect transistors of the cascodes serving as the second input means and being, in operation, connected directly to the first voltage supply.

[0008] The amplifier is especially suitable for operation where the difference between the first voltage supply and second voltage supply is less than 2.5 volts.

[0009] Preferably, the amplifier comprises:

a first n-channel transistor including an input gate terminal for receiving a first input signal,
a second n-channel transistor including an input gate for receiving a second input signal,
the source terminals of said first and second n-channel transistors being connected together and, in operation, connected to the first voltage supply,
a third n-channel transistor including a source terminal to which the drain terminal of said first n-channel transistor is coupled,
a fourth n-channel transistor including a source terminal to which the drain of said second n-channel transistor is

coupled,
the gate terminals of said third and fourth n-channel transistors being connected together and for receiving a first common mode control signal,
a first p-channel transistor including a drain terminal to which the drain terminal of said third n-channel transistor and a first input of said common mode adjust circuit are connected, the drain terminals of the transistors serving as a first differential signal output terminal,
a second p-channel transistor including a drain terminal to which the drain terminal of said fourth n-channel transistor and a second input of said common mode adjust circuit are connected, the drain terminals of the transistors serving as a second differential signal output terminal,
the gate terminals of said first and second p-channel transistors being connected together for receiving a second common mode control signal,
a third p-channel transistor including a drain terminal to which the source terminal of said first p-channel transistor is connected,
a fourth p-channel transistor including a drain terminal to which the source terminal of said second p-channel transistor is connected,
the gate terminals of said third and fourth p-channel transistors connected together for receiving a first output signal from said common mode adjust circuit,
the source terminals of said third and fourth p-channel connected together for connection to the second voltage supply and
a second output terminal of said common mode adjust circuit providing an over-range voltage output signal.

[0010] Preferably, the operational amplifier further comprises:

a correction voltage generator circuit and
a summing amplifier circuit together arranged to monitor the common mode output signal from the common mode adjust circuit and the amplifier being capable of:

monitoring the common mode output signal,
comparing the common mode output signal to a specified range around said amplifier's nominal bias current,
generating an out-of-range error signal when the monitored output signal is above or below said specified range, and
making with the correction voltage generator circuit and the summing amplifier circuit an appropriate correction to the operational amplifier's common mode input voltage when said specified range is exceeded.

[0011] Preferably, the amplifier includes:

an input terminal of said correction voltage generator is coupled to an output terminal of said common mode adjust circuit,
an output of said correction voltage generator is coupled to a first input of said summing amplifier,
a second input to said summing amplifier is coupled to a common mode voltage and
an output of said summing amplifier provides the corrected common mode input voltage to said amplifier.

[0012] Preferably, the amplifier comprises:

means for generating a common mode feedback signal;
means for establishing replicas of the amplifier common mode currents;
means for generating UP and DOWN counter control signals by comparing replica common mode currents to upper and lower current limits; and
means for providing a corrected input common mode voltage using an UP/DOWN counter, a digital-to-analog converter, and summing circuit to develop a small correction current which is summed to the nominal amplifier bias current.

[0013] Preferably, the amplifier further comprises:

means coupling a positive differential output of said operational amplifier to the gate of a first n-channel transistor;
means coupling the negative differential output of said operational amplifier to the gate of a second n-channel transistor;
means coupling the output common mode voltage to the gate of a third n-channel transistor;

the sources of said first, second, and third n-channel transistors being connected together and coupled to the input of a current source;
means coupling the output of said current source to circuit ground;
the drains of said first and second n-channel transistors being connected together and coupled to the gate and drain of a first p-channel transistor and to the gate of a second p-channel transistor;
the source of said first p-channel transistor being coupled to the source of said second p-channel transistor, to the drain of a fourth n-channel transistor, and to the power supply voltage;
the drain of said second p-channel transistor being coupled to the source and gate of said fourth n-channel transistor, to the drain of said third n-channel transistor, and to the common mode feedback signal output.

[0014] Preferably, the amplifier further comprises:

means coupling the common mode feedback signal to the gates of a first and a second p-channel transistor;
the sources of said first and second p-channel transistors being connected together and coupled to the power supply source;
the drain of said first p-channel transistor being coupled to the input of a first current source and to the under range signal output;
the drain of said second p-channel transistor being coupled to the input of a second current source and to the over range signal output;
the outputs of said first and second current sources being connected together and coupled to circuit ground.

[0015] Preferably, the amplifier includes an UP/DOWN counter, a digital-to-analog converter, and summing circuitry to develop a small correction current which is summed to the nominal amplifier bias current, further comprising:

an under range input voltage coupled to the input of an inverter;
the output of said inverter being coupled to the first input of an UP/DOWN counter;
an over range input voltage coupled to the second input of said UP/DOWN counter;
a clock signal coupled to the third input of said UP/DOWN counter;
the output of said UP/DOWN counter being coupled to the input of a digital-to-analog (D/A) converter;
the output of said D/A converter being coupled to the gate and drain of a n-channel transistor, to the output of a current source, and to the input common mode voltage output;
the input of said current source being coupled to the power supply voltage;
the source of said n-channel transistor being coupled to circuit ground.

[0016] The amplifier may include a charge pump circuit and a capacitor in place of the combination of said UP/DOWN counter and digital-to-analog converter.

[0017] Preferably, the amplifier comprises:

means for replicating the current flowing in the input transistors of the main operational amplifier and generating UP and DOWN counter control signals by comparing replica currents to the upper and lower current limits;
means for providing a corrected input common mode voltage using an UP/DOWN counter, a digital-to-analog converter, and summing circuitry to develop a small correction current which is summed to the nominal amplifier bias current.

[0018] Preferably, the amplifier replicates the current flowing in the input transistors of the main operational amplifier and generates UP and DOWN counter control signals by comparing replica currents to the upper and lower current limits, comprising:

a positive differential input signal coupled to the negative input of said operational amplifier of this patent and to the gates of a first and a second n-channel transistor;
a negative differential input signal coupled to the positive input of said operational amplifier and to the gates of a third and a fourth n-channel transistor;
the sources of said first and third n-channel transistors being connected together and coupled to circuit ground;
the sources of said second and fourth n-channel transistors being connected together and coupled to circuit ground;
the drains of said first and third n-channel transistors being connected together and coupled to the output of a first current source and to an under range voltage output;
the drains of said second and fourth n-channel transistors being connected together and coupled to the output of a second current source and to an over range voltage output;

the inputs to said first and second current sources being connected together and coupled to the power supply source;
the positive differential output of said amplifier being coupled to the circuit's positive signal output;
the negative differential output of said amplifier being coupled to the circuit's negative signal output.

[0019] Preferably, the amplifier provides a corrected input common mode input voltage using an UP/DOWN counter, a digital-to-analog converter, and summing circuitry to develop a small correction current which is summed to the nominal amplifier bias current, comprising:

an under range input voltage coupled to the input of an inverter;
the output of said inverter being coupled to the first input of an UP/DOWN counter;
an over range input voltage coupled to the second input of said UP/DOWN counter;
a clock signal coupled to the third input of said UP/DOWN counter;
the output of said UP/DOWN counter being coupled to the input of a digital-to-analog (D/A) converter;
the output of said D/A converter being coupled to the gate and drain of a n-channel transistor, to the output of a current source, and to the input common mode voltage output;
the input of said current source being coupled to the power supply voltage;
the source of said n-channel transistor being coupled to circuit ground.

[0020] A switched capacitor amplifier, advantageously, includes an amplifier in accordance with the invention connected to a network of capacitors and switches.

[0021] Preferably, the switched capacitor amplifier further comprises:

said first differential input signal coupled to the input of a first phase 1 switch;
said second differential input signal coupled to the input of a second phase 1 switch;
the output of said first phase 1 switch coupled to the input of a first phase 2 switch and to the bottom plate of a first capacitor;
the output of said second phase 1 switch coupled to the input of a second phase 2 switch and to the bottom plate of a second capacitor;
the outputs of said first and second phase 1 switches connected together and coupled to the common mode output voltage;
the top plate of said first capacitor coupled to top plate of a third capacitor, to the input of a third phase 1 switch, and to the negative input of said operational amplifier;
the top plate of said second capacitor coupled to the top plate of a fourth capacitor, to the input of a fourth phase 1 switch, and to the positive input of said operational amplifier;
the outputs of said third and fourth phase 1 switches connected together and coupled to the input common mode voltage;
the bottom plate of said third capacitor coupled to input of a third phase 2 switch and to the input of a fifth phase 1 switch;
the bottom plate of said fourth capacitor coupled to input of a fourth phase 2 switch and to the input of a sixth phase 1 switch;
the output of said fifth and sixth phase 1 switches coupled to the output common mode voltage;
the positive differential output of said operational amplifier coupled to the output of said third phase 2 switch and to the first input of common mode adjust circuit;
the negative differential output of said operational amplifier coupled to the output of said fourth phase 2 switch and to the second input of said common mode adjust circuit;
the first output of said common mode adjust circuit coupled to the third input of said operational amplifier;
the second output of said common mode adjust circuit providing an over range voltage used for the common mode correction.

[0022] The invention provides a method for generating an operational amplifier common mode input correction voltage, comprising:

generating a common mode feedback signal;
establishing replicas of the amplifier common mode currents;
generating UP and DOWN counter control signals by comparing replica common mode currents to upper and lower current limits; and
providing a corrected input common mode voltage using an UP/DOWN counter, a digital-to-analog converter, and

summing circuit to develop a small correction current which is summed to the nominal amplifier bias current.

[0023] An apparatus for generating an operational amplifier common mode input correction voltage, comprises:

means for generating a common mode feedback signal;
means for establishing replicas of the amplifier common mode currents;
means for generating UP and DOWN counter control signals by comparing replica common mode currents to upper and lower current limits; and
means for providing a corrected input common mode voltage including an UP/DOWN counter, a digital-to-analog converter, and summing circuit to develop a small correction current which is summed to the nominal amplifier bias current.

[0024] Preferably, the apparatus generates a common mode feedback signal and further comprises:

a positive differential output of said operational amplifier coupled to the gate of a first n-channel transistor;
the negative differential output of said operational amplifier coupled to the gate of a second n-channel transistor;
the output common mode voltage coupled to the gate of a third n-channel transistor;
the sources of said first, second, and third n-channel transistors connected together and coupled to the input of a current source;
the output of said current source coupled to circuit ground;
the drains of said first and second n-channel transistors connected together and coupled to the gate and drain of a first p-channel transistor and to the gate of a second p-channel transistor;
the source of said first p-channel transistor coupled to the source of said second p-channel transistor, to the drain of a fourth n-channel transistor, and to the power supply voltage;
the drain of said second p-channel transistor coupled to the source and gate of said fourth n-channel transistor, to the drain of said third n-channel transistor, and to the common mode feedback signal output.

[0025] Preferably, the apparatus establishes replicas of the amplifier common mode current and generates counter control signals by comparing replica common mode currents to upper and lower limits, further comprising:

the common mode feedback signal being coupled to the gates of a first and a second p-channel transistor;
the sources of said first and second p-channel transistors being connected together and coupled to the power supply source;
the drain of said first p-channel transistor being coupled to the input of a first current source and to the under range signal output;
the drain of said second p-channel transistor being coupled to the input of a second current source and to the over range signal output;
the outputs of said first and second current sources being connected together and coupled to circuit ground.

[0026] Preferably, the apparatus provides a corrected common mode input voltage using an UP/DOWN counter, a digital-to-analog converter, and summing circuitry to develop a small correction current which is summed to the nominal amplifier bias current, further comprising:

an under range input voltage coupled to the input of an inverter;
the output of said inverter being coupled to the first input of an UP/DOWN counter;
an over range input voltage coupled to the second input of said UP/DOWN counter;
a clock signal coupled to the third input of said UP/DOWN counter;
the output of said UP/DOWN counter being coupled to the input of a digital-to-analog (D/A) converter;
the output of said D/A converter being coupled to the gate and drain of a n-channel transistor, to the output of a current source, and to the input common mode voltage output;
the input of said current source being coupled to the power supply voltage;
the source of said n-channel transistor being coupled to circuit ground.

[0027] Preferably, the apparatus provides said corrected common mode input voltage by replacing the combination of said UP/DOWN counter and digital-to-analog converter with a charge pump and a capacitor, respectively.

[0028] An alternative for generating an operational amplifier common mode input correction voltage, comprises:

replicating the current flowing in the input transistors of the main operational amplifier and generates UP and

DOWN counter control signals by comparing replica currents to the upper and lower current limits;
providing a corrected input common mode voltage using an UP/DOWN counter, a digital-to-analog converter, and summing circuitry to develop a small correction current which is summed to the nominal amplifier bias current.

[0029] An alternative apparatus for generating an operational amplifier common mode input correction voltage, comprises:

means for replicating the current flowing in the input transistors of the main operational amplifier and generates UP and DOWN counter control signals by comparing replica currents to the upper and lower current limits;
means for providing a corrected input common mode voltage using an UP/DOWN counter, a digital-to-analog converter, and summing circuitry to develop a small correction current which is summed to the nominal amplifier bias current.

[0030] Preferably, the apparatus replicates the current flowing in the input transistors of the main operational amplifier and generates UP and DOWN counter control signals by comparing replica currents to the upper and lower current limits, comprising:

a positive differential input signal coupled to the negative input of said operational amplifier of this patent and to the gates of a first and a second n-channel transistor;
a negative differential input signal coupled to the positive input of said operational amplifier and to the gates of a third and a fourth n-channel transistor;
the sources of said first and third n-channel transistors connected together and coupled to circuit ground;
the sources of said second and fourth n-channel transistors connected together and coupled to circuit ground;
the drains of said first and third n-channel transistors connected together and coupled to the output of a first current source and to an under range voltage output;
the drains of said second and fourth n-channel transistors connected together and coupled to the output of a second current source and to an over range voltage output;
the inputs to said first and second current sources connected together and coupled to the power supply source;
the positive differential output of said operational amplifier coupled to the circuit's positive signal output;
the negative differential output of said operational amplifier coupled to the circuit's negative signal output.

[0031] Preferably, the apparatus provides a corrected input common mode input voltage using an UP/DOWN counter, a digital-to-analog converter, and summing circuitry to develop a small correction current which is summed to the nominal amplifier bias current, comprising:

an under range input voltage coupled to the input of an inverter;
the output of said inverter coupled to the first input of an UP/DOWN counter;
an over range input voltage coupled to the second input of said UP/DOWN counter;
a clock signal coupled to the third input of said UP/DOWN counter;
the output of said UP/DOWN counter coupled to the input of a digital-to-analog (D/A) converter;
the output of said D/A converter coupled to the gate and drain of a n-channel transistor, to the output of a current source, and to the input common mode voltage output;
the input of said current source coupled to the power supply voltage;
the source of said n-channel transistor coupled to circuit ground.

[0032] A switched capacitor operational amplifier, may comprise:

a differential cascoded input transistor pair coupled to first and second input signals;
active transistor loads for each said input transistor;
a common mode adjust circuit;
a common mode input voltage correction generator; with the sources of said input transistors coupled directly to a supply voltage thereby eliminating a long tail current source.

[0033] Preferably, the switched capacitor operational amplifier further comprises:

said first differential input signal coupled to the input of a first phase 1 switch;
said second differential input signal coupled to the input of a second phase 1 switch;
the output of said first phase 1 switch coupled to the input of a first phase 2 switch and to the bottom plate of a

first capacitor;
the output of said second phase 1 switch coupled to the input of a second phase 2 switch and to the bottom plate of a second capacitor;
the outputs of said first and second phase 1 switches connected together and coupled to the common mode output voltage;
the top plate of said first capacitor coupled to top plate of a third capacitor, to the input of a third phase 1 switch, and to the negative input of said operational amplifier;
the top plate of said second capacitor coupled to the top plate of a fourth capacitor, to the input of a fourth phase 1 switch, and to the positive input of said operational amplifier;
the outputs of said third and fourth phase 1 switches connected together and coupled to the input common mode voltage;
the bottom plate of said third capacitor coupled to input of a third phase 2 switch and to the input of a fifth phase 1 switch;
the bottom plate of said fourth capacitor coupled to input of a fourth phase 2 switch and to the input of a sixth phase 1 switch;
the output of said fifth and sixth phase 1 switches coupled to the output common mode voltage;
the positive differential output of said operational amplifier coupled to the output of said third phase 2 switch and to the first input of common mode adjust circuit;
the negative differential output of said operational amplifier coupled to the output of said fourth phase 2 switch and to the second input of said common mode adjust circuit;
the first output of said common mode adjust circuit coupled to the third input of said operational amplifier;
the second output of said common mode adjust circuit providing an over range voltage used for the common mode correction.

[0034] A new differential, low voltage, broadband operational amplifier which eliminates the long tail current source from the amplifier, thereby relieving the low voltage headroom requirements, is disclosed. This advantage will allow the amplifier to operate from a power supply of less than 2.5 volts.

[0035] The circuitry of this invention compensates for the significant changes in drain current in the input transistors of the amplifier by monitoring the current in a common mode feedback signal. When the value of this current exceeds a specified range around the nominal amplifier bias current, an appropriate correction is made to the common mode input voltage. Using this circuitry which can be implemented with minimal chip area and negligible power consumption, an operational amplifier is built without a long tail current source that operates at voltages of 2.5 volts or less.

[0036] Two implementations for the control loop for common mode input voltage are discussed, although other implementations are possible. Simulated results for both a conventional amplifier and the operational amplifier of this invention, both running from a power supply of less than 2.5 volts, are compared.

[0037] The included drawings are as follows:

Figure 1	shows a circuit diagram for a conventional telescopic cascode operational amplifier. (prior art)
Figure 2	depicts the schematic for a first embodiment of the modified telescopic cascode operational amplifier of this invention.
Figures 3a and 3b	is the schematic and clock cycle, respectively, for a typical switched capacitor amplifier using the operational amplifier of Figure 2.
Figures 4a and 4b	are block diagrams for the common mode input voltage correction technique used with the operational amplifier of this invention in both (a) the switched capacitor and (b) other general applications.
Figures 5a, 5b, and 5c	are schematic diagrams for a first implementation of the common mode voltage correction technique of Figure 4.
Figure 6	is a schematic diagram for a second implementation of the common mode input voltage correction technique of Figure 4.
Figure 7	compares simulation results for the operational amplifier of this invention and for a conventional cascode operational amplifier, both running from a 2.5 volt power supply.

[0038] Figure 2 is a schematic for a first embodiment of the modified operational amplifier circuit 11 with common mode adjust circuitry 10, which addresses the low voltage headroom problem discussed in the earlier prior art discussion. Here, the long tail current source 5 (in Figure 1) has been eliminated completely, taking away the common mode rejection properties of the amplifier. As in Figure 1, this differential op-amp is comprised of cascoded n-channel input transistors 1,3 and 2,4 at the V_{ip} and V_{in} inputs, respectively, but with the long tail current source transistor 5 (Figure

1) eliminated. P-channel transistors 6-9 act as an active load. The common mode adjust circuitry 10 is used to compensate for any change in the common mode input voltage of the operational amplifier 11. As before, the differential outputs V_{Op} and V_{On} for the circuit are taken from the drains of n-channel transistors 3 and 4, respectively. As long as the common mode input voltage (V_{CMI} in Figure 3a) is kept equal to or appoximately equal to one transistor V_{GS} drop, this circuit can still be used as an operational amplifier. There are a number of applications where this circuit can be used, for example a fully differential switched-capacitor circuit often used in pipelined analog-to-digital converters, where there is little need for a high common-mode-rejection-ratio (CMRR) since all inputs and outputs are referenced to highly regulated internal bias voltages. This circuit requires a headroom which is 0.3V to 0.5 V smaller than the conventional long tail operational amplifier circuit of Figure 1. However, in a general sense, if the input common mode voltage is different from the desired value, the drain current of input transistors 1 and 2 can exhibit large variations from their nominal values. One simple solution to this problem is to increase the range of the output common mode adjustment circuitry 10 such that the current in transistors 8 and 9 can accommodate the current variation in input transistors 1 and 2 and make the necessary corrections. However, this can result in large undesirable variations in the amplifier bandwidth, making it desirable to have a more sophisticated, higher performance approach to the common mode input voltage correction problem.

[0039] Figure 3a is a schematic diagram for a switched-capacitor amplifier using the operational amplifier of the first embodiment of this invention. This circuit is chosen to illustrate the reasons why the common mode input voltage, V_{CMI}, changes. The circuit is comprised of the operational amplifier 11 of this invention, common mode adjust circuitry 10, four switched capacitors 12-15, phase 1 switches 16-21, and phase 2 switches 22-25, and has differential inputs V_{ip} and V_{in} and differential outputs V_{op} and V_{on}. A clock cycle, consisting of phase 1 (p_1) sampling phase and phase 2 (p_2) amplification phase, for the circuit is shown in Figure 3b. The operation of the circuit is as follows. During phase 1, when p_1 switches 16-21 are closed, the top plates of all capacitors 12-15 (C_1 - C_4) are connected to the input common mode voltage V_{CMI}, whereas the bottom plates of capacitors 12 and 13 ($C_1$and C_2) are connected to V_{ip} and V_{in}, respectively, and the bottom plates of capacitors 14 and 15 (C_3 and C_4) are connected to the output common mode voltage V_{CMO}. Ideally, the common voltage of V_{ip} and V_{in} would be the same as V_{CMO}, as a result of the common mode feedback circuit of the previous stage. Then during phase 2, the bottom plates of capacitors 14 and 15 (C_3 and C_4) are connected to outputs V_{op} and V_{on}, respectively, while the bottom plates of capacitors 12 and 13 ($C_1$and C_2) are connected to V_{CMO}. Again, under ideal conditions, the common mode voltage at the amplifier input would be unchanged from phase 1 to phase 2. However, in practice the common mode voltages of V_{ip}, V_{in} and V_{op}, V_{on} are different from V_{CMO} due to the non-idealities in the common mode feedback circuit of the preceding stage. This results in a change in the common mode input voltage of the amplifier during phase 2.

[0040] Another possible source of error is that of signal feed-through from the switches that are used for connecting the amplifier input nodes to V_{CMI} during phase 1. This can result in a change in the input common mode voltage V_{CMI} during phase 2. The combination of all these error sources can cause the common mode input voltage to change on the order of several tens of millivolts, which in turn can cause the drain current in input transistors 1 and 2 to change by as much as 25%, or more.

[0041] Figure 4 shows the method for correcting the common mode input voltage variations for this embodiment of the invention. Figure 4a illustrates this input common mode correction for the switched-capacitor amplifier 26 application discussed earlier, while Figure 4b shows this correction for a general-case amplifier application. In both cases (Figure 4a and Figure 4b) the amount of current supplied to amplifier 11 by the common mode feedback (CMFB) signal is monitored inside the common mode adjust circuit 10. Whenever this current exceeds a certain range, say ± 10% of the nominal amplifier bias current, an over-range or under-range signal is generated by the common mode adjust circuitry 10. This is then used to apply a suitable correction to the V_{CMI} voltage by means of a correction voltage generator 27 and summing circuit 28. This second correction feedback loop must be made slower that the main CMFB loop in order to avoid any signal 'chatter'.

[0042] A first technique for correcting the common mode input voltage variations of this invention is shown in Figure 5. Figure 5a shows the common mode feedback circuit which generates the V_{CMFB} signal. This circuit is comprised on one side of two n-channel transistors 29-30 for input signals V_{OP} and V_{ON}, respectively, a current source 31, and a diode connected p-channel transistor 32. The other side of the circuit is comprised of a n-channel transistor 33 for the V_{CMO} input signal, a diode connected n-channel transistor 34, and the same current source 31. Another p-channel transistor 35 couples the two sides of the circuit together. The inputs to the circuit are V_{OP}, V_{ON}, and V_{CMO} and the output is V_{CMFB}.

[0043] The circuit of Figure 5b consists of two current mirrors, each comprised of a p-channel transistor 36 and/or 38 and a current source 37 and/or 39. This circuit monitors the V_{CMFB} signal and generates two replicas of the common mode current supplied to the main amplifier. These currents are then compared with a lower current limit I_{UR} and a higher current limit I_{OR}, flowing in constant current sources 37 and 39, respectively. If the current in the I_{OR} leg of the circuit exceeds the constant current I_{OR}, then the V_{OR} output signal will go high (UP). Likewise, if the current in the I_{UR} leg of the circuit is less than the constant current I_{UR}, then the V_{UR} output signal will go low (DOWN).

[0044] These V_{OR} and V_{UR} signals are then fed into the correction circuitry of Figure 5c. In this circuit, the V_{UR} signal is complemented by means of an inverter 40 and fed into the UP input of an UP/DOWN counter 41, while the V_{OR} signal is feed into the DOWN input of the same UP/DOWN counter 41. The counter 41 drives a low resolution (3-to-4 bits) digital-to-analog (D/A) converter 42 which generates a small correction current that is added to or subtracted from the current flowing in current source 43, which represents the nominal amplifier bias current. This total current is fed into a diode connected n-channel (M_{BIAS}) transistor 44 that is matched with the input transistors 1 and 2 of the main amplifier 11, shown in Figure 2. In operation, the operational amplifier's output signals V_{OP} and V_{ON} are compared with the common mode output voltage V_{CMO} and an appropriate common mode feedback signal V_{CMFB} is generated. Any change in the V_{CMFB} signal is reflected at the output of the current mirrors as an increase or decrease in the V_{OR} and V_{UR} signals, respectively. These V_{OR} and V_{UR} signals are then used to make the counter count clock pulsed either UP or DOWN. Finally, the output of the counter is converted back to an analog current and is added to or subtracted from the amplifier's nominal current and used to adjust the V_{CMI} voltage, such as to maintain common mode between the operational amplifier's input and output signals. In practice, the circuitry associated with this correction implementation can be realized with a small amount of extra chip area and a negligible amount of power. The combination of the UP/DOWN counter and D/A converter can also be implemented using a charge pump and a capacitor.

[0045] A second technique for implementing the control loop for the common mode input voltage correction of this invention is shown in Figure 6. Here, the combinations of two n-channel transistors pairs 45-46 and 47-48 are used to replicate the current flowing in the input transistors 1 and 2 of the main amplifier 11. These are compared with reference currents I_{UR}, which is slightly smaller than the nominal current, and I_{OR}, which is slightly larger than the nominal current, that is flowing in the I_{UR} current source 49 and the I_{OR} current source 50, respectively. If the replicated current is outside of the established window for the I_{UR} and I_{OR} currents, a correction is applied to the V_{CMI} using the same UP/DOWN counter circuit of Figure 5c.

[0046] Figure 7 compares the simulation results for both a conventional operational amplifier and the new operational amplifier of this patent, both running from a 2.5 volt power supply. As shown, for a given input signal, a several tenths of volt improvement in the output amplitude is realized, making it a desired circuit for low voltage applications.

[0047] While this invention has been described in the context of a preferred embodiment, it will be apparent to those skilled in the art that the present invention may be modified in numerous ways and may assume many embodiments other than that specifically set out and described above. Accordingly, it is intended by the appended claims to cover all modifications of the invention which fall within the true spirit and scope of the invention.

Claims

1. A differential operational amplifier for operation between a first and a second voltage supply, comprising:

   a differential pair of cascoded input transistors including first input means for receiving first and second input signals,
   active transistor loads for connecting output means of each of said input transistor cascodes to the second voltage supply, and
   a common mode adjust circuit connected to adjust the currents in the active transistor loads in accordance with the common mode output signal from the output means of the differential pair of cascoded input transistors, wherein

   in the operation of the amplifier, second input means of said cascoded input transistors are coupled directly to the first voltage supply.

2. An amplifier as claimed in claim 1, including field effect transistors in the differential pair of cascoded input transistors, the source terminals of the lower (1,2) field effect transistors of the cascodes serving as the second input means and being, in operation, connected directly to the first voltage supply.

3. An amplifier as claimed in claim 1 or claim 2, wherein the difference between the first voltage supply and second voltage supply is less than 2.5 volts.

4. An amplifier as claimed in any one of claims 1 to 3, comprising:

   a first n-channel transistor including an input gate terminal for receiving a first input signal,
   a second n-channel transistor including an input gate for receiving a second input signal,
   the source terminals of said first and second n-channel transistors being connected together and, in operation,

connected to the first voltage supply,
a third n-channel transistor including a source terminal to which the drain terminal of said first n-channel transistor is coupled,
a fourth n-channel transistor including a source terminal to which the drain of said second n-channel transistor is coupled,
the gate terminals of said third and fourth n-channel transistors being connected together and for receiving a first common mode control signal,
a first p-channel transistor including a drain terminal to which the drain terminal of said third n-channel transistor and a first input of said common mode adjust circuit are connected, the drain terminals of the transistors serving as a first differential signal output terminal,
a second p-channel transistor including a drain terminal to which the drain terminal of said fourth n-channel transistor and a second input of said common mode adjust circuit are connected, the drain terminals of the transistors serving as a second differential signal output terminal,
the gate terminals of said first and second p-channel transistors being connected together for receiving a second common mode control signal,
a third p-channel transistor including a drain terminal to which the source terminal of said first p-channel transistor is connected,
a fourth p-channel transistor including a drain terminal to which the source terminal of said second p-channel transistor is connected,
the gate terminals of said third and fourth p-channel transistors connected together for receiving a first output signal from said common mode adjust circuit,
the source terminals of said third and fourth p-channel connected together for connection to the second voltage supply and
a second output terminal of said common mode adjust circuit providing an over-range voltage output signal.

5. An operational amplifier as claimed in any one of claims 1 to 4, further comprising:

a correction voltage generator circuit and
a summing amplifier circuit together arranged to monitor the common mode output signal from the common mode adjust circuit and the amplifier being capable of:

monitoring the common mode output signal,
comparing the common mode output signal to a specified range around said amplifier's nominal bias current,
generating an out-of-range error signal when the monitored output signal is above or below said specified range, and
making with the correction voltage generator circuit and the summing amplifier circuit an appropriate correction to the operational amplifier's common mode input voltage when said specified range is exceeded.

6. An amplifier as claimed in claim 5, wherein:

an input terminal of said correction voltage generator is coupled to an output terminal of said common mode adjust circuit,
an output of said correction voltage generator is coupled to a first input of said summing amplifier,
a second input to said summing amplifier is coupled to a common mode voltage and
an output of said summing amplifier provides the corrected common mode input voltage to said amplifier.

7. An amplifier as claimed in claim 5 or claim 6, comprising:

means for generating a common mode feedback signal;
means for establishing replicas of the amplifier common mode currents;
means for generating UP and DOWN counter control signals by comparing replica common mode currents to upper and lower current limits; and
means for providing a corrected input common mode voltage using an UP/DOWN counter, a digital-to-analog converter, and summing circuit to develop a small correction current which is summed to the nominal amplifier bias current.

8. An amplifier as claimed in any one of claims 5 to 7, further comprising:

means coupling a positive differential output of said operational amplifier to the gate of a first n-channel transistor;
means coupling the negative differential output of said operational amplifier to the gate of a second n-channel transistor;
means coupling the output common mode voltage to the gate of a third n-channel transistor;
the sources of said first, second, and third n-channel transistors being connected together and coupled to the input of a current source;
means coupling the output of said current source to circuit ground;
the drains of said first and second n-channel transistors being connected together and coupled to the gate and drain of a first p-channel transistor and to the gate of a second p-channel transistor;
the source of said first p-channel transistor being coupled to the source of said second p-channel transistor, to the drain of a fourth n-channel transistor, and to the power supply voltage;
the drain of said second p-channel transistor being coupled to the source and gate of said fourth n-channel transistor, to the drain of said third n-channel transistor, and to the common mode feedback signal output.

9. An amplifier as claimed in any one of claims 5 to 8, further comprising:

means coupling the common mode feedback signal to the gates of a first and a second p-channel transistor;
the sources of said first and second p-channel transistors being connected together and coupled to the power supply source;
the drain of said first p-channel transistor being coupled to the input of a first current source and to the under range signal output;
the drain of said second p-channel transistor being coupled to the input of a second current source and to the over range signal output;
the outputs of said first and second current sources being connected together and coupled to circuit ground.

10. An amplifier as claimed in any one of claims 5 to 9, including an UP/DOWN counter, a digital-to-analog converter, and summing circuitry to develop a small correction current which is summed to the nominal amplifier bias current, further comprising:

an under range input voltage coupled to the input of an inverter;
the output of said inverter being coupled to the first input of an UP/DOWN counter;
an over range input voltage coupled to the second input of said UP/DOWN counter;
a clock signal coupled to the third input of said UP/DOWN counter;
the output of said UP/DOWN counter being coupled to the input of a digital-to-analog (D/A) converter;
the output of said D/A converter being coupled to the gate and drain of a n-channel transistor, to the output of a current source, and to the input common mode voltage output;
the input of said current source being coupled to the power supply voltage;
the source of said n-channel transistor being coupled to circuit ground.

11. An amplifier as claimed in claim 10, including a charge pump circuit and a capacitor in place of the combination of said UP/DOWN counter and digital-to-analog converter.

12. An amplifier as claimed in claim 5 or claim 6, comprising:

means for replicating the current flowing in the input transistors of the main operational amplifier and generating UP and DOWN counter control signals by comparing replica currents to the upper and lower current limits;
means for providing a corrected input common mode voltage using an UP/DOWN counter, a digital-to-analog converter, and summing circuitry to develop a small correction current which is summed to the nominal amplifier bias current.

13. An amplifier as claimed in claim 12, which replicates the current flowing in the input transistors of the main operational amplifier and generates UP and DOWN counter control signals by comparing replica currents to the upper and lower current limits, comprising:

a positive differential input signal coupled to the negative input of said operational amplifier of this patent and to the gates of a first and a second n-channel transistor;
a negative differential input signal coupled to the positive input of said operational amplifier and to the gates

of a third and a fourth n-channel transistor;
the sources of said first and third n-channel transistors being connected together and coupled to circuit ground;
the sources of said second and fourth n-channel transistors being connected together and coupled to circuit ground;
the drains of said first and third n-channel transistors being connected together and coupled to the output of a first current source and to an under range voltage output;
the drains of said second and fourth n-channel transistors being connected together and coupled to the output of a second current source and to an over range voltage output;
the inputs to said first and second current sources being connected together and coupled to the power supply source;
the positive differential output of said amplifier being coupled to the circuit's positive signal output;
the negative differential output of said amplifier being coupled to the circuit's negative signal output.

14. An amplifier as claimed in claim 12 or claim 13, which provides a corrected input common mode input voltage using an UP/DOWN counter, a digital-to-analog converter, and summing circuitry to develop a small correction current which is summed to the nominal amplifier bias current, comprising:

an under range input voltage coupled to the input of an inverter;
the output of said inverter being coupled to the first input of an UP/DOWN counter;
an over range input voltage coupled to the second input of said UP/DOWN counter;
a clock signal coupled to the third input of said UP/DOWN counter;
the output of said UP/DOWN counter being coupled to the input of a digital-to-analog (D/A) converter;
the output of said D/A converter being coupled to the gate and drain of a n-channel transistor, to the output of a current source, and to the input common mode voltage output;
the input of said current source being coupled to the power supply voltage;
the source of said n-channel transistor being coupled to circuit ground.

15. A switched capacitor amplifier including an amplifier as claimed in any one of claims 1 to 14 connected to a network of capacitors and switches.

16. The switched capacitor amplifier as claimed in claim 15, further comprising:

said first differential input signal coupled to the input of a first phase 1 switch;
said second differential input signal coupled to the input of a second phase 1 switch;
the output of said first phase 1 switch coupled to the input of a first phase 2 switch and to the bottom plate of a first capacitor;
the output of said second phase 1 switch coupled to the input of a second phase 2 switch and to the bottom plate of a second capacitor;
the outputs of said first and second phase 1 switches connected together and coupled to the common mode output voltage;
the top plate of said first capacitor coupled to top plate of a third capacitor, to the input of a third phase 1 switch, and to the negative input of said operational amplifier;
the top plate of said second capacitor coupled to the top plate of a fourth capacitor, to the input of a fourth phase 1 switch, and to the positive input of said operational amplifier;
the outputs of said third and fourth phase 1 switches connected together and coupled to the input common mode voltage;
the bottom plate of said third capacitor coupled to input of a third phase 2 switch and to the input of a fifth phase 1 switch;
the bottom plate of said fourth capacitor coupled to input of a fourth phase 2 switch and to the input of a sixth phase 1 switch;
the output of said fifth and sixth phase 1 switches coupled to the output common mode voltage;
the positive differential output of said operational amplifier coupled to the output of said third phase 2 switch and to the first input of common mode adjust circuit;
the negative differential output of said operational amplifier coupled to the output of said fourth phase 2 switch and to the second input of said common mode adjust circuit;
the first output of said common mode adjust circuit coupled to the third input of said operational amplifier;
the second output of said common mode adjust circuit providing an over range voltage used for the common mode correction.

17. A method for generating an operational amplifier common mode input correction voltage, comprising:

generating a common mode feedback signal;
establishing replicas of the amplifier common mode currents;
generating UP and DOWN counter control signals by comparing replica common mode currents to upper and lower current limits; and
providing a corrected input common mode voltage using an UP/DOWN counter, a digital-to-analog converter, and summing circuit to develop a small correction current which is summed to the nominal amplifier bias current.

18. An apparatus for generating an operational amplifier common mode input correction voltage, comprising:

means for generating a common mode feedback signal;
means for establishing replicas of the amplifier common mode currents;
means for generating UP and DOWN counter control signals by comparing replica common mode currents to upper and lower current limits; and
means for providing a corrected input common mode voltage including an UP/DOWN counter, a digital-to-analog converter, and summing circuit to develop a small correction current which is summed to the nominal amplifier bias current.

19. An apparatus as claimed in claim 18, which generates a common mode feedback signal, further comprising:

a positive differential output of said operational amplifier coupled to the gate of a first n-channel transistor;
the negative differential output of said operational amplifier coupled to the gate of a second n-channel transistor;
the output common mode voltage coupled to the gate of a third n-channel transistor;
the sources of said first, second, and third n-channel transistors connected together and coupled to the input of a current source;
the output of said current source coupled to circuit ground;
the drains of said first and second n-channel transistors connected together and coupled to the gate and drain of a first p-channel transistor and to the gate of a second p-channel transistor;
the source of said first p-channel transistor coupled to the source of said second p-channel transistor, to the drain of a fourth n-channel transistor, and to the power supply voltage;
the drain of said second p-channel transistor coupled to the source and gate of said fourth n-channel transistor, to the drain of said third n-channel transistor, and to the common mode feedback signal output.

20. An apparatus as claimed in claim 18 or claim 19, which establishes replicas of the amplifier common mode current and generates counter control signals by comparing replica common mode currents to upper and lower limits, further comprising:

the common mode feedback signal being coupled to the gates of a first and a second p-channel transistor;
the sources of said first and second p-channel transistors being connected together and coupled to the power supply source;
the drain of said first p-channel transistor being coupled to the input of a first current source and to the under range signal output;
the drain of said second p-channel transistor being coupled to the input of a second current source and to the over range signal output;
the outputs of said first and second current sources being connected together and coupled to circuit ground.

21. An apparatus as claimed in any one of claims 18 to 20, which provides a corrected common mode input voltage using an UP/DOWN counter, a digital-to-analog converter, and summing circuitry to develop a small correction current which is summed to the nominal amplifier bias current, further comprising:

an under range input voltage coupled to the input of an inverter;
the output of said inverter being coupled to the first input of an UP/DOWN counter;
an over range input voltage coupled to the second input of said UP/DOWN counter;
a clock signal coupled to the third input of said UP/DOWN counter;
the output of said UP/DOWN counter being coupled to the input of a digital-to-analog (D/A) converter;

the output of said D/A converter being coupled to the gate and drain of a n-channel transistor, to the output of a current source, and to the input common mode voltage output;
the input of said current source being coupled to the power supply voltage;
the source of said n-channel transistor being coupled to circuit ground.

22. An apparatus as claimed in any one of claims 18 to 21, which provides said corrected common mode input voltage by replacing the combination of said UP/DOWN counter and digital-to-analog converter with a charge pump and a capacitor, respectively.

23. A method for generating an operational amplifier common mode input correction voltage, comprising:

replicating the current flowing in the input transistors of the main operational amplifier and generates UP and DOWN counter control signals by comparing replica currents to the upper and lower current limits;
providing a corrected input common mode voltage using an UP/DOWN counter, a digital-to-analog converter, and summing circuitry to develop a small correction current which is summed to the nominal amplifier bias current.

24. An apparatus for generating an operational amplifier common mode input correction voltage, comprising:

means for replicating the current flowing in the input transistors of the main operational amplifier and generates UP and DOWN counter control signals by comparing replica currents to the upper and lower current limits;
means for providing a corrected input common mode voltage using an UP/DOWN counter, a digital-to-analog converter, and summing circuitry to develop a small correction current which is summed to the nominal amplifier bias current.

25. An apparatus as claimed in claim 24, which replicates the current flowing in the input transistors of the main operational amplifier and generates UP and DOWN counter control signals by comparing replica currents to the upper and lower current limits, comprising:

a positive differential input signal coupled to the negative input of said operational amplifier of this patent and to the gates of a first and a second n-channel transistor;
a negative differential input signal coupled to the positive input of said operational amplifier and to the gates of a third and a fourth n-channel transistor;
the sources of said first and third n-channel transistors connected together and coupled to circuit ground;
the sources of said second and fourth n-channel transistors connected together and coupled to circuit ground;
the drains of said first and third n-channel transistors connected together and coupled to the output of a first current source and to an under range voltage output;
the drains of said second and fourth n-channel transistors connected together and coupled to the output of a second current source and to an over range voltage output;
the inputs to said first and second current sources connected together and coupled to the power supply source;
the positive differential output of said operational amplifier coupled to the circuit's positive signal output;
the negative differential output of said operational amplifier coupled to the circuit's negative signal output.

26. An apparatus as claimed in claim 24 or 25, which provides a corrected input common mode input voltage using an UP/DOWN counter, a digital-to-analog converter, and summing circuitry to develop a small correction current which is summed to the nominal amplifier bias current, comprising:

an under range input voltage coupled to the input of an inverter;
the output of said inverter coupled to the first input of an UP/DOWN counter;
an over range input voltage coupled to the second input of said UP/DOWN counter;
a clock signal coupled to the third input of said UP/DOWN counter;
the output of said UP/DOWN counter coupled to the input of a digital-to-analog (D/A) converter;
the output of said D/A converter coupled to the gate and drain of a n-channel transistor, to the output of a current source, and to the input common mode voltage output;
the input of said current source coupled to the power supply voltage;
the source of said n-channel transistor coupled to circuit ground.

27. A switched capacitor operational amplifier, comprising:

a differential cascoded input transistor pair coupled to first and second input signals;
active transistor loads for each said input transistor;
a common mode adjust circuit;
a common mode input voltage correction generator; with the sources of said input transistors coupled directly to a supply voltage thereby eliminating a long tail current source.

28. A switched capacitor operational amplifier as claimed in claim 27, further comprising:

said first differential input signal coupled to the input of a first phase 1 switch;
said second differential input signal coupled to the input of a second phase 1 switch;
the output of said first phase 1 switch coupled to the input of a first phase 2 switch and to the bottom plate of a first capacitor;
the output of said second phase 1 switch coupled to the input of a second phase 2 switch and to the bottom plate of a second capacitor;
the outputs of said first and second phase 1 switches connected together and coupled to the common mode output voltage;
the top plate of said first capacitor coupled to top plate of a third capacitor, to the input of a third phase 1 switch, and to the negative input of said operational amplifier;
the top plate of said second capacitor coupled to the top plate of a fourth capacitor, to the input of a fourth phase 1 switch, and to the positive input of said operational amplifier;
the outputs of said third and fourth phase 1 switches connected together and coupled to the input common mode voltage;
the bottom plate of said third capacitor coupled to input of a third phase 2 switch and to the input of a fifth phase 1 switch;
the bottom plate of said fourth capacitor coupled to input of a fourth phase 2 switch and to the input of a sixth phase 1 switch;
the output of said fifth and sixth phase 1 switches coupled to the output common mode voltage;
the positive differential output of said operational amplifier coupled to the output of said third phase 2 switch and to the first input of common mode adjust circuit;
the negative differential output of said operational amplifier coupled to the output of said fourth phase 2 switch and to the second input of said common mode adjust circuit;
the first output of said common mode adjust circuit coupled to the third input of said operational amplifier;
the second output of said common mode adjust circuit providing an over range voltage used for the common mode correction.

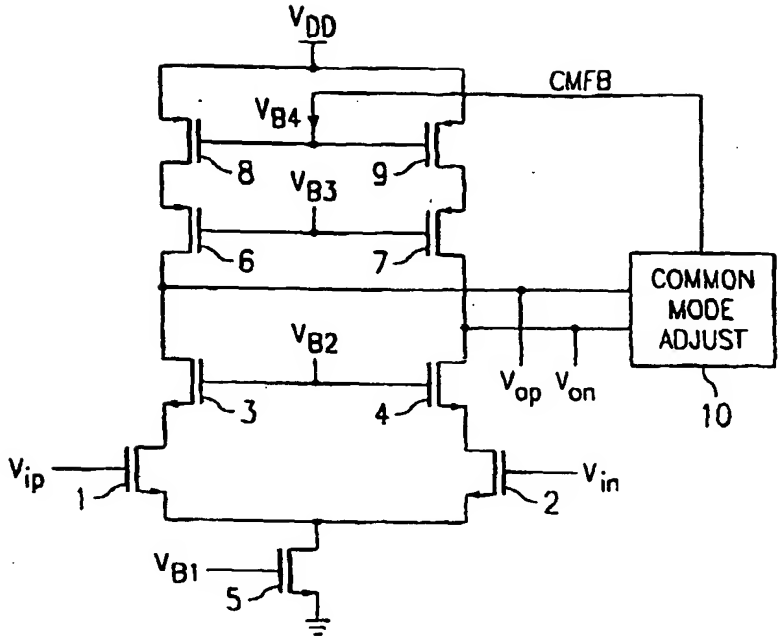

FIG. 1
(PRIOR ART)

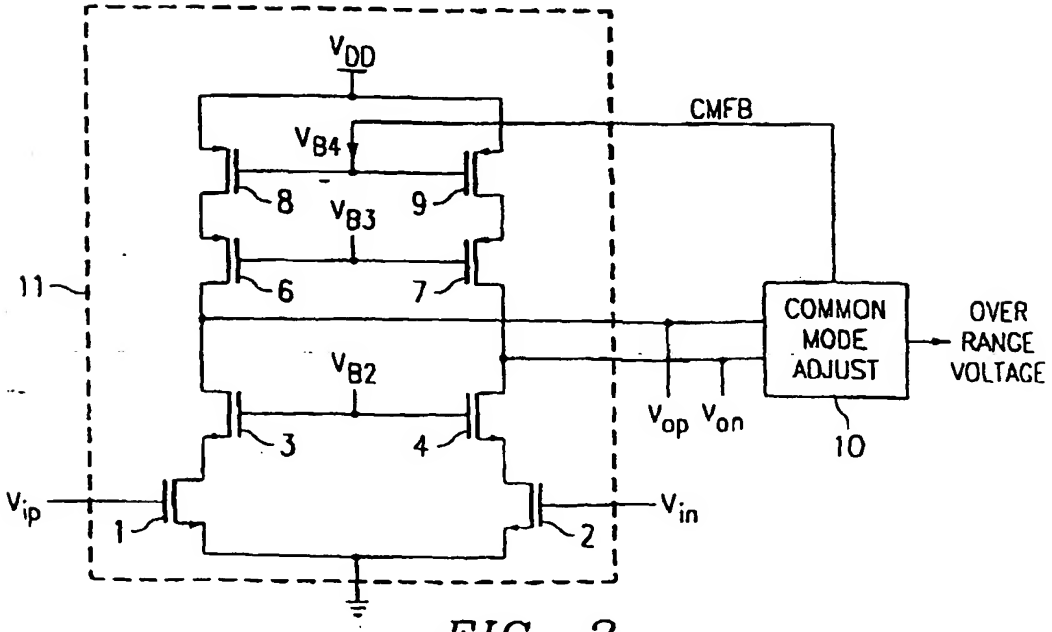

FIG. 2

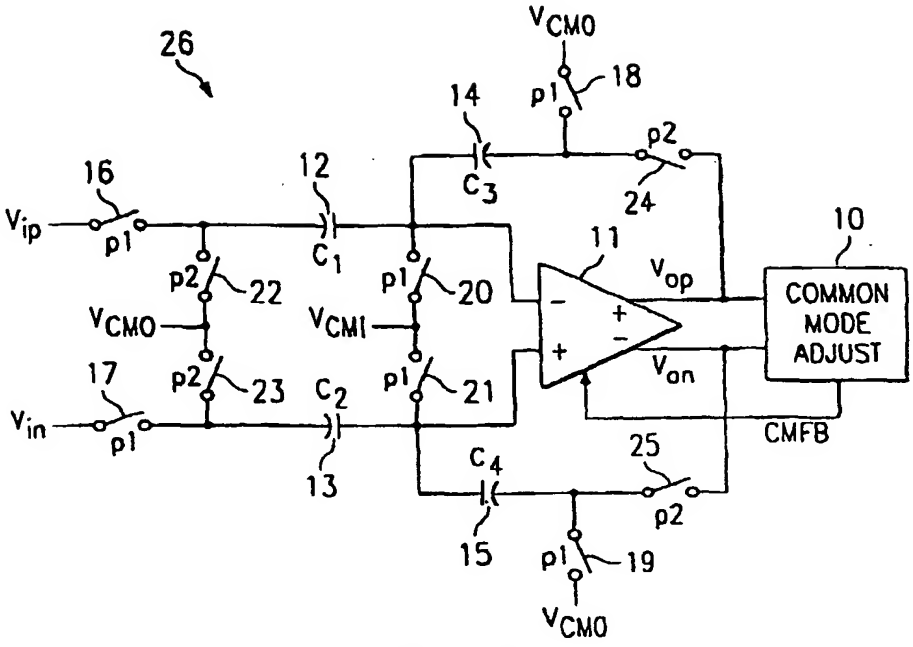
26
V_{CMO}
18
p1
14
p2
16
12
C_3
24
V_{ip}
p1
C_1
11
10
p2
22
p1
20
V_{op}
COMMON MODE ADJUST
V_{CMO}
V_{CMI}
17
p2
23
C_2
p1
21
V_{on}
V_{in}
p1
CMFB
C_4
25
13
p2
15
p1
19
V_{CMO}

FIG. 3a

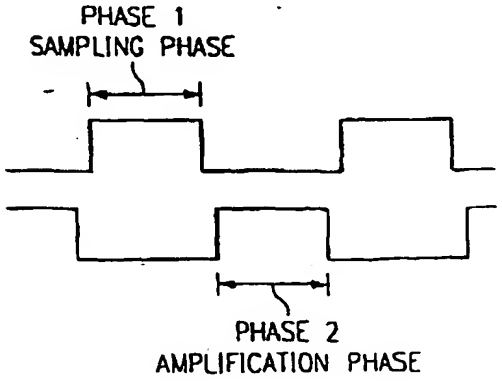
PHASE 1
SAMPLING PHASE
PHASE 2
AMPLIFICATION PHASE

FIG. 3b

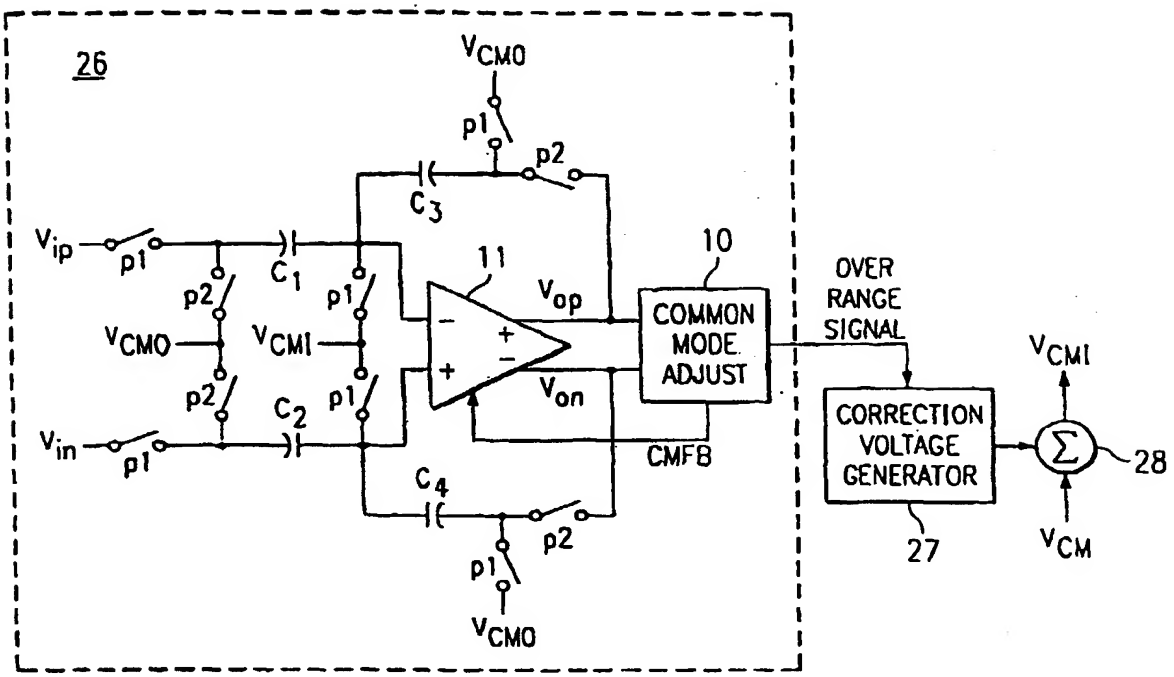

FIG. 4a

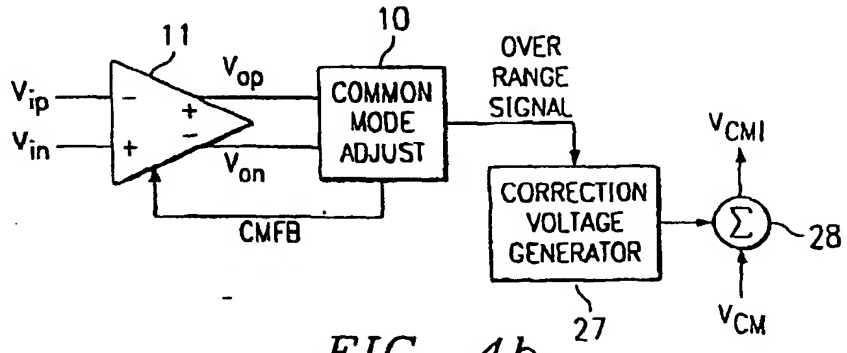

FIG. 4b

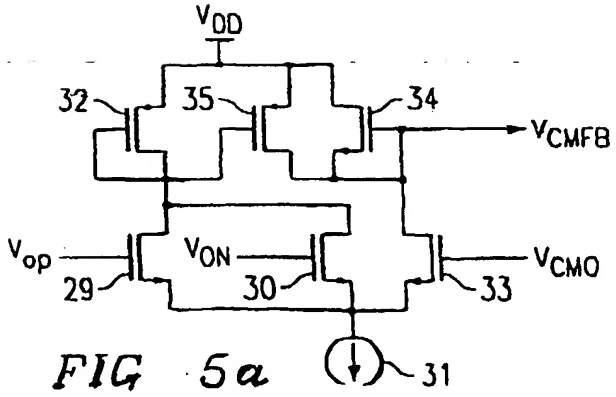

FIG 5a

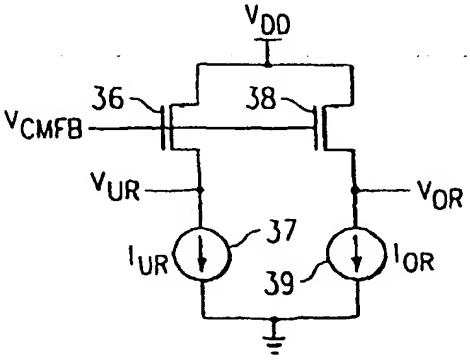

FIG. 5b

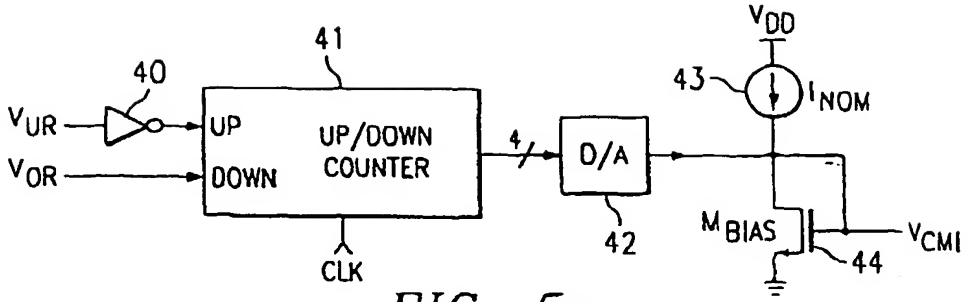

FIG. 5c

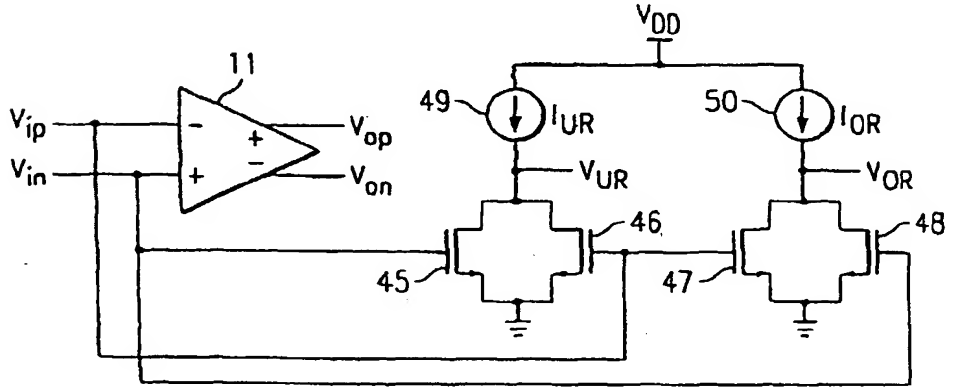

FIG. 6

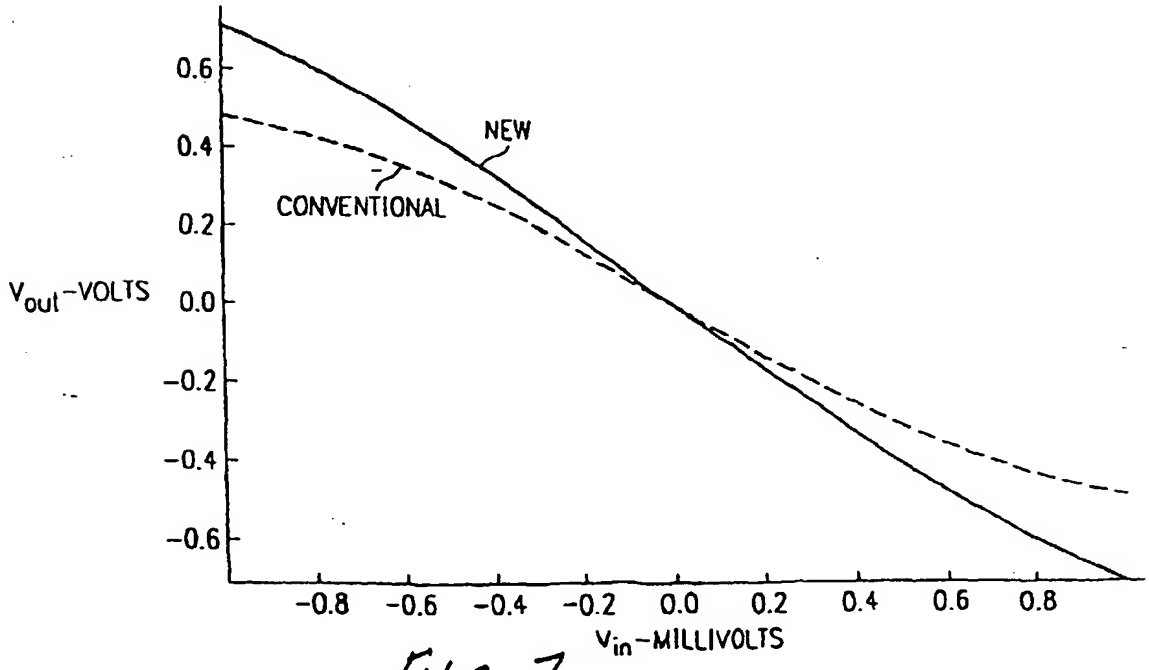

FIG. 7

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 00 30 9405

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
Y	ADACHI T ET AL: "A LOW NOISE INTEGRATED AMPS IF FILTER" PROCEEDINGS OF THE CUSTOM INTEGRATED CIRCUITS CONFERENCE,US,NEW YORK, IEEE, vol. CONF. 16, 1 May 1994 (1994-05-01), pages 159-162, XP000492875	1,2	H03F3/45
A	* page 160 - page 161; figure 3 *	4-6,8,9, 20	

Y	US 4 656 436 A (SAARI VEIKKO R) 7 April 1987 (1987-04-07)	1,2	
A	* abstract; figure 1 *	4,8	

Y	REZZI F ET AL: "A 3V PSEUDO-DIFFERENTIAL TRANSCONDUCTOR WITH INTRINSIC REJECTION OFTHE COMMON-MODE INPUT SIGNAL" PROCEEDINGS OF THE MIDWEST SYMPOSIUM ON CIRCUITS AND SYSTEMS,US,NEW YORK, IEEE, vol. SYMP. 37, 3 August 1994 (1994-08-03), pages 85-88, XP000531982 ISBN: 0-7803-2429-3	1,2	
A	* page 86 - page 87; figure 4 *	4,8	TECHNICAL FIELDS SEARCHED (Int.Cl.7)
	---		H03F
A	US 5 914 638 A (HE XINPING) 22 June 1999 (1999-06-22) * abstract; figure 3 *	15,16, 27,28	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	12 February 2001	Tyberghien, G

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4656436 A	07-04-1987	CA 1238693 A	28-06-1988
		EP 0228843 A	15-07-1987
		JP 62166606 A	23-07-1987
US 5914638 A	22-06-1999	NONE	

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